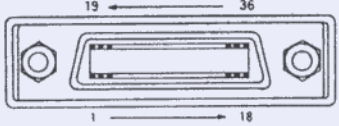
5.1 Pin Arrangement

The BCD OUT Connector has the following pin arrangement:

Pin No.	Signal Contents		Pin No.	Signal Contents
1	$1x10^0$	BCD output	19	$4x10^4$
2	$2x10^0$		20	$8x10^4$
3	$4x10^0$		21	LOWER output
4	$8x10^0$		22	OK output
5	$1x10^1$	BCD output	23	UPPER output
6	$2x10^1$		24	N.C
7	$4x10^1$		25	Polarity output +
8	$8x10^1$		26	Polarity output -
9	$1x10^2$	BCD output	27	D.P3 decimal point output
10	$2x10^2$		28	D.P4 decimal point output
11	$4x10^2$		29	N.C
12	$8x10^2$		30	Error output
13	$1x10^3$	BCD output	31	HOLD input
14	$2x10^3$		32	RESET input
15	$4x10^3$		33	BUSY input
16	$8x10^3$		34	COMPARATOR GATE input
17	$1x10^4$	BCD output	35	Print command output
18	$2x10^4$		36	Common

Receptacle : DX10A-36S (Hirose Electric Co.)
Applicable plug : DX40-36P (Hirose Electric Co.)
Plug cover : DX36-CV1 (Hirose Electric Co.)



5.2 Signals

① BCD Output
- Pin 1 to Pin 20
- Positive/negative logic change 5-digit parallel output
- Open collector output

② Pass-fail Decision Result Output
- Pin 21 (LOWER output): ON when LOWER set value ≥ Measured value
- Pin 22 (OK output): ON when LOWER set value < Measured value < UPPER set value
- Pin 23 (UPPER output): ON when UPPER set value ≤ Measured value
- Open collector output

③ Polarity Output
- Pin 25 (+ output)
- Pin 26 (- output)
- Open collector output
- Polarity output turns ON/OFF as shown in the table on the following page when Bit Switch 3 (BCD OUT) in the main unit is set to ON to select the negative logic.
  When Bit Switch 3 is set to OFF to select the positive logic, polarity output ON/OFF is all reversed.

Pin / Measured Value	25 (+ Output)	26 (- Output)
Positive (+) value	ON	OFF
Negative (-) value	OFF	ON
Reset	ON	OFF

④ Decimal Point Output

- Pin 27 (D.P3, when Bit Switch 1 (SENSOR) in the main unit is set to OFF to select the resolution of 10 μm)
- Pin 28 (D.P4, when Bit Switch 1 (SENSOR) in the main unit is set to ON to select the resolution of 1 μm)
- Decimal point output turns ON/OFF as shown in the following table when Bit Switch 3 (BCD OUT) in the main unit is set to ON to select the negative logic.
  When Bit Switch 3 is set to OFF to select the positive logic, polarity output ON/OFF is all reversed.

Pin / Resolution	27(D.P3)	28(D.P4)
1 μm (Bit Switch 1 ON)	OFF	ON
10 μm (Bit Switch 1 OFF)	ON	OFF

⑤ Error Output
- Pin 30
- Open collector output
- When miscounting occurs in the counting circuit of the DG-4240, the ON signal is output; which is continued until reset.

⑥ HOLD Input
- Pin 31
- When a low level voltage signal is input, the displayed value and BCD output are held and the print command signal is output.
- While the low level signal is input, the HOLD state is continued. However, counting is still operated in the counting circuit according to the input signal from the gauge sensor while the HOLD state is retained. Therefore, when the HOLD state is released, the displayed value and BCD output are changed to a value measured at that time.

⑦ RESET Input
- Pin 32
- When a low level voltage signal is input, the displayed value, BCD output, error indication, and error output are reset. While the low level signal is input, the RESET state is continued.

⑧ BUSY Input
- Pin 33
- Same as ⑥ HOLD Input

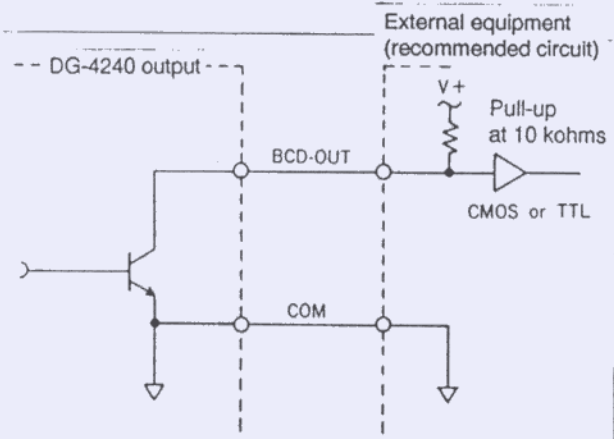
⑨ COMPARATOR GATE Input
- Pin 34
- When a low level voltage signal is input, the pass-fail decision is forcedly stopped to set all decision result outputs to OFF.

⑩ Print Command Output
- Pin 35
- Open collector output
- When the HOLD or BUSY signal is input to hold the displayed value and BCD output, the negative pulse print command signal is output.

5.3 Recommended Interface

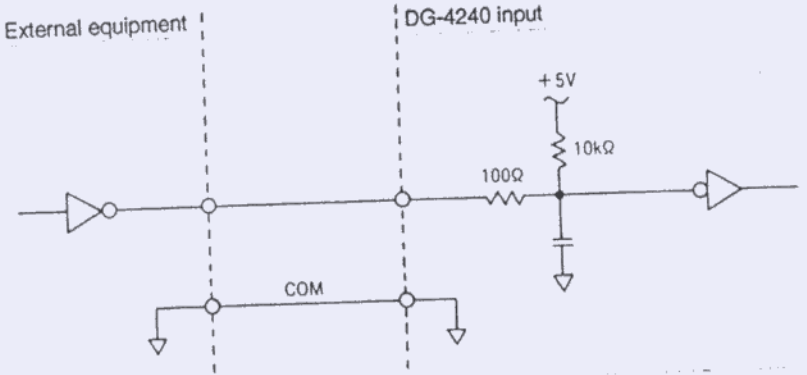
Verify that the external equipment connected to the BCD OUT Connector on the rear panel has the interface circuits described below. For the recommended interface for external command signal input from the terminal block, see page *6-1*.

Output signal interface circuit (BCD OUT Connector)



Output Type	Open collector output
Output IC	74LS07
Voltage resistance	24 V max
Max. synch current	32 mA max
Residual voltage	0.5 V max

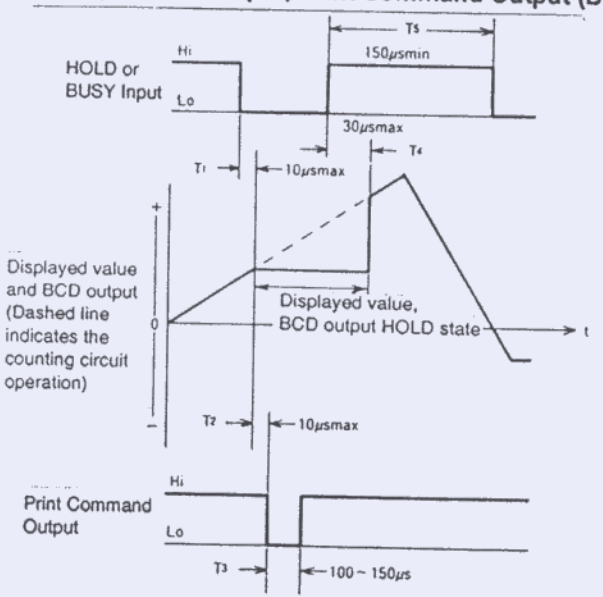
Input signal interface circuit (BCD OUT Connector)



Low level input voltage	0 ~ 1.4V
High level input voltage	3 ~ 5.25 V
Input impedance	1 kohm or more

5.4 Timing Chart

■ HOLD Input, BUSY Input, Print Command Output (BCD OUT Connector)



T_1: Time from HOLD signal input to HOLD state of the displayed value and BCD output; max. 10 μs.

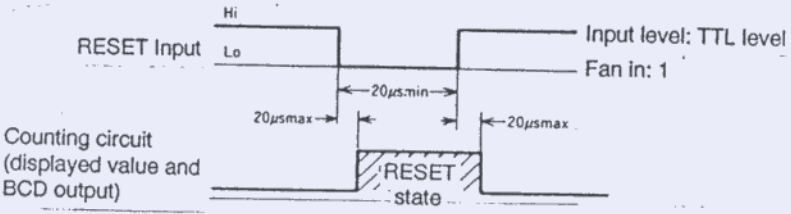
T_2: Time from HOLD state of the displayed value and BCD output to print command signal output; max. 10 μs.

T_3: Print command signal pulse width; 100 t 150 μs.

T_4: Time from HOLD signal release to HOLI state release; max. 30 μs.

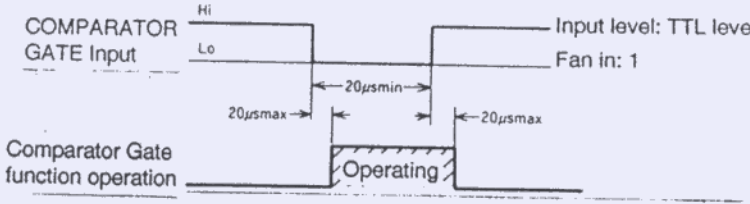
T_5: Time from HOLD signal release to HOLI signal reinput; min. 150 μs. If the HOLD signal is input at an interval shorter than 150 μs, the print command signal may not be output.

■ RESET Input (BCD OUT Connector)



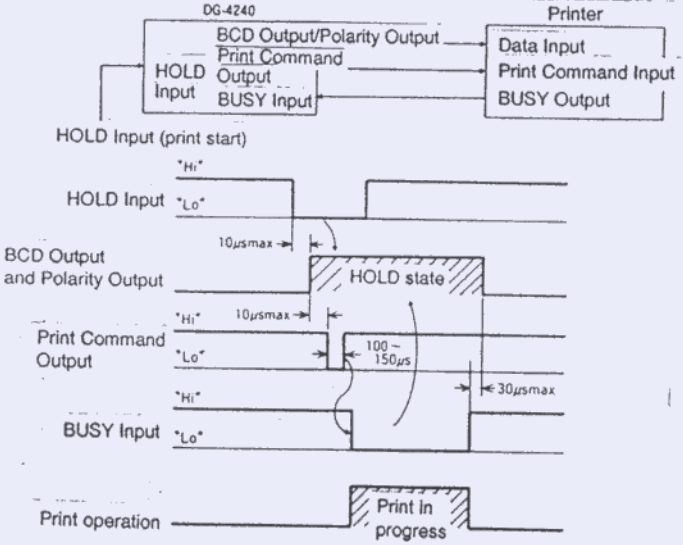
The RESET signal must have a pulse width of minimum 20 μs. It takes up to 20 μs from RESET signal input to RESET state and from RESET signal release to RESET state release, respectively.

■ COMPARATOR GATE Input (BCD OUT Connector)



The COMPARATOR GATE signal must have a pulse width of minimum 20 μs. It takes up to 20 μs from COMPARATOR GATE signal input to its functional operation start and from COMPARATOR GATE signal release to function release, respectively.

■ Print Command Output (BCD OUT Connector)

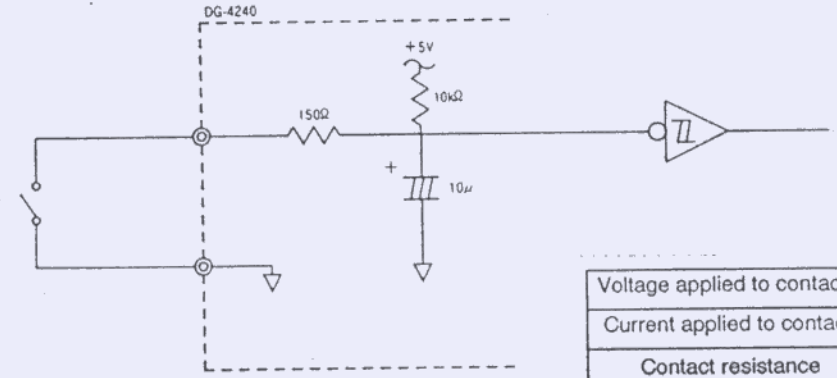


This timing chart shows that the printer is started at the rising of the print command signal. Retain the HOLD Input at the low level until the BUSY Input becomes the low level.

6.1 Recommended Interface

■ Input signal interface circuit (terminal block)

Verify that the external equipment connected to the COMPARATOR GATE Input Terminal, HOLD Input Terminal, and RESET Input Terminal on the rear panel of the DG-4240 has the interface circuit shown below.

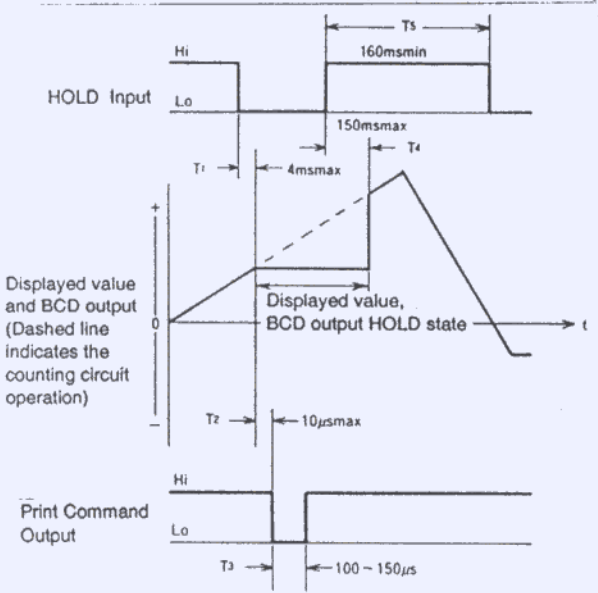


Voltage applied to contact	DC5 V ± 0.25 V
Current applied to contact	50mA max
Contact resistance	100 ohms or less

At 0 to 40 deg.C

6.2 Timing Chart

■ HOLD Input, Print Command Output (Terminal Block)



T_1: Time from HOLD signal input to HOLD state of the displayed value and BCD Output; max. 4 ms.

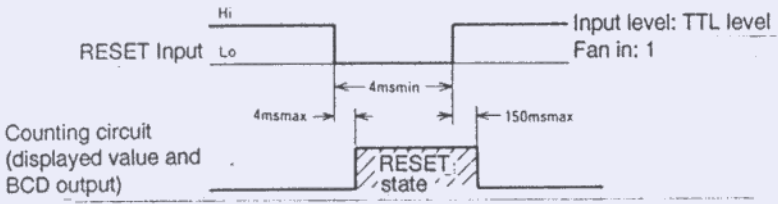
T_2: Time from HOLD state of the displayed value and BCD Output to print command signal output; max. 10 μs.

T_3: Print command signal pulse width; 100 to 150 μs.

T_4: Time from HOLD signal release to HOLD state release; max. 150 μs.

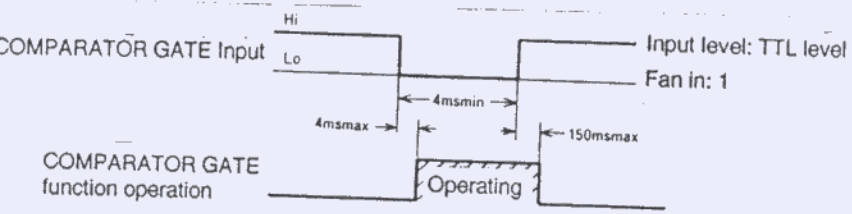
T_5: Time from HOLD signal release to HOLD signal reinput; min. 160 ms. If the HOLD signal is input at an interval shorter than 150 μs, the print command signal may not be output.

■ RESET Input (Terminal Block)



The RESET signal must have a pulse width of minimum 4 ms. It takes up to 4 ms from RESET signal input to RESET state. It takes up to 150 ms from RESET signal release to RESET state release.

■ COMPARATOR GATE Input (Terminal Block)



The COMPARATOR GATE signal must have a pulse width of minimum 4 ms. It takes up to 4 ms from COMPARATOR GATE signal input to its functional operation start. It takes up to 150 ms from COMPARATOR GATE signal release to functional release.